Instruction Cycle

Er. Anshu Singh

Assistant Professor

Computer Science & Engineering Department

University of Lucknow

Lucknow

Branch: BCA

Semester: 3

Subject: Computer Architecture

Disclaimer: The e-content is exclusively meant for academic purposes and for enhancing teaching and learning. Any other use for economic/commercial purpose is strictly prohibited. The users of the content shall not distribute, disseminate or share it with anyone else and its use is restricted to advancement of individual knowledge. The information provided in this e-content is developed from authentic references, to the best of my knowledge.

Instruction Cycle

A program that exists inside a computer's memory unit consists of a series of instructions. The processor executes these instructions through a cycle for each instruction.

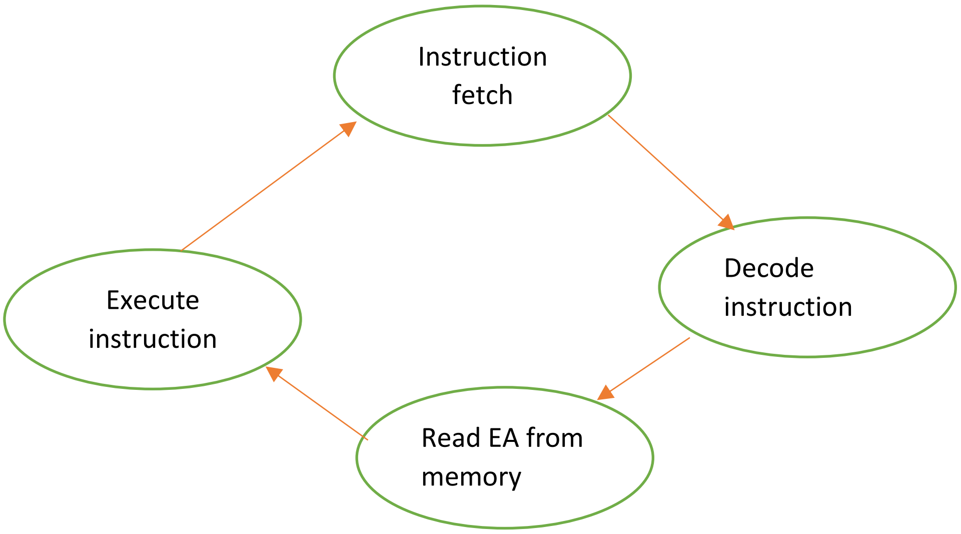
In a basic computer, each instruction cycle consists of the following phases:

Instruction fetch: fetch instruction from memory

Decode the instruction: what operation to be performed.

Read the effective address from memory

Execute the instruction



Registers Involved In Each Instruction Cycle:

Memory address registers(MAR) : It is connected to System Bus address lines. It specifies the address of a read or write operation in memory.

Memory Buffer Register(MBR) : It is connected to the data lines of the system bus. : It is connected to the system bus Data Lines. It holds the memory value to be stored, or the last value read from the memory.

Program Counter(PC) : Holds the address of the next instruction to be fetched.

Instruction Register(IR) : Holds the last instruction fetched.

Fetch cycle

The address of the next instruction to execute is in the Program Counter(PC) at the beginning of the fetch cycle.

Step 1: The address in the program counter is transferred to the Memory Address Register(MAR), as this is the only register that is connected to the system bus address lines.

Step 2: The address in MAR is put on the address bus, now a Read order is provided by the control unit on the control bus, and the result appears on the data bus and is then copied into the memory buffer register. Program counter is incremented by one, to get ready for the next instruction. These two acts can be carried out concurrently to save time.

Step 3: The content of the MBR is moved to the instruction register(IR).

Instruction fetch cycle consist of four micro operation:

T1: MAR← PC

T2: MBR← memory

PC← PC + stepsize or length of instruction

T3: IR← MBR

Decode instruction cycle

The next move is to fetch source operands once an instruction is fetched. Indirect addressing (it can be obtained by any addressing mode, here it is done by indirect addressing) is obtained by Source Operand. You don't need to fetch register-based operands. If the opcode is executed, it will require a similar process to store the result in main memory. Micro-operations take place:

T1: MAR← IR(address)

T2: MBR← Memory

T3: IR(address)← (MBR(Address))

Step 1: The instruction address field is passed to the MAR. This is used to fetch the operand 's address.

Step 2: The address field of the IR is updated from the MBR.

Step 3: The IR is now in the state. Now IR is ready for the execute cycle.

Execute instruction Cycle

The initial three cycles (Fetch, Indirect, and Interrupt) are predictable and quick. Each requires simple , small, and fixed micro-operation sequences. The same micro-operation is repeated every time around in each event. Execute instruction cycle is different from them. Like, there is N different series of micro-operations that can occur for a computer with different N opcodes.

Example

ADD R , X

T1: MAR← (IR(address))

T2: MBR← Memory

T3: R← (R) + (MBR)

Step 1: The address portion of IR is loaded into the MAR.
Step 2: The address field of the IR is updated from the MBR, so the reference memory location is read.
Step 3: Now, the contents of R and MBR are added by the ALU.

References:

1. John P Hayes "Computer Architecture and organization" McGraw Hill
2. Dezso Sima,Terence Fountain and Peter Kacsuk " Advanced Computer Architecture" Pearson Education
3. Kai Hwang " Advanced Computer Architecture" TMH
4. Linda Null, Julia Lobur- The Essentials of Computer Organization and Architecture, 2014, 4th Edition.